TRIPLE TRACK DELTA ASIC
WITH SHIFT-OUT
3 VOLT

SPECIFICATIONS

Specification Part Number 99875337 Rev 9

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REVISIONS

Rev	Date	Description
1	15 Jan 06	Initial Release
2	7 Feb 06	Fixed Specification Tables. Added notes about dual head setup and JEDEC soldering recommendations. Updated schematic example.
3	4 Apr 06	Electrical Characteristics, p.16, Vdd Time Constant, changed min value from 4 to 6 us. To note 1 after “if necessary”, added “to meet the 6us minimum time-constant requirement.”
4	2 Jun 06	Corrected errors in references to figure numbers; corrected figures 9 and 10
5	3 Oct 06	Added warning about power-up sequence. Added TstbH_CP timing constraint
6	25 Oct 06	Corrected timing diagram typo whereby TstbH_CP was shown replacing every instance of TstbH instead of just one as intended
7	23 Oct 07	Corrected Electrical Characteristics diagram to show V input high in the Min. column and V input low in the Max. column
8	13 Jan 09	Added MTBF specification
9	7 Aug 13	Replaced latest drawings that show IC marking changes.

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INTRODUCTION

MagTek is pleased to offer a new version of our high-performance low-cost three-channel fully integrated magnetic stripe decoder chip or ASIC (Application Specific Integrated Circuit). This new version offers better economy with added features. Still packaged in a 14 pin MLFTM (MicroLeadFrameTM), this new ASIC provides backwards compatibility while adding an easier reset function, a larger data buffer, lower power, and indefinite memory retention.

In addition to the 14 pin MLF™ Packaged Triple-Track ASIC as a stand-alone chip, MagTek also offers the Shift-Out IntelliHead, a magnetic head with the chip actually built-in. The Shift-Out IntelliHead uses the same Triple-Track ASIC, but completely encapsulated in a low-profile magnetic head, offering further integration and excellent noise immunity by shielding the low-level analog signals inside the head. Unless your application dictates the use of a particular separate or custom magnetic head, MagTek recommends the Shift-Out IntelliHead for best performance, best miniaturization, and best economy. See MagTek specification 99875258 for information on the Shift-Out IntelliHead.

Backwards compatible with MagTek's 21006536/37 and 21006529/39 Triple Track ASICs[1]

- **Low cost solution for single, dual, or triple track readers** – one triple-track chip works for all
- **Compact design –** 4 mm x 5 mm, 14 pin MLFTM (also called QFN) surface mount package
- **Minimal external components** – only a decoupling capacitor is required. Only 2 signals, **DATA**, and **STROBE**, to connect to your micro-controller for up to 3 tracks
- **Data buffer with Shift-Out** – allows full card data to be locally stored on ASIC. Retrieve when desired. Use a low-cost controller with no interrupts, limited memory, low-speed, low pin-count, etc.
- **Robust re-synchronization capabilities** – reads cards with badly damaged leading or synchronization zero-bits in either swipe direction
- **High noise immunity** – with proper PCB layout, the ASIC can withstand noisy PC monitors, cell phones, switching power supplies, etc.
- **High performance decoding** – reads badly damaged cards; compensates for poor head mounting
- **Card-Present Feature** – indicates when an encoded card is being swiped
- **Low voltage operation** – 2.7 V to 3.6 V
- **Low operating current** – less than 1 mA total current at 3.3V (for up to 3 tracks) while card is being swiped

[1] See MagTek Specification 99875259 for the 21006536/37 and 99875336 for the 21006529/39 ASICs for further details.

- **Low Armed-to-Read current** – less than 120 μA total current when no card is being swiped and the device is armed to read
- **Even lower OFF state current –** less than 10 μA when device is held in the OFF state and less than 20 μA in the Shift-Out or Data Extraction state (185 μA in backwards-compatible "Old Mode")

- **Ideal for ultra-low-power applications –** supports systems where the micro-controller and ASIC are not both in a high-current state simultaneously but for short periods of time

- **AGC (Automatic Gain Control)** – reads cards from 30% - 200% of International Standards Organization (ISO) 7811 amplitude standard

- **Wide operational temperature range** – -40° C to +85° C

- **Wide range of card swipe speeds** – from 2 to 100 in/s (5 to 254 cm/s) for the standard 75 to 210 bits per inch (bpi) data density

- **ROHS Compliant** – "lead (Pb) free" component

CONFIGURATIONS

Part Number	Description
21006540	ASIC, Triple Track, F/2F Decode, 3V, MLF14, Tube
21006541	ASIC, Triple Track, F/2F Decode, 3V, MLF14, Tape and Reel

OPERATION – NEW MODE

The ASIC features two user-selected modes, Old Mode and New Mode. Old Mode offers backwards compatibility with MagTek's 21006536/37 and 21006529/39 ASICs. See OPERATION – OLD MODE for details. New Mode offers an increased memory size and unlimited cycling through the data buffer. New Mode is recommended for new designs.

For backwards compatibility, the ASIC powers up in Old Mode by default. A reset must be initiated to enter New Mode. To initiate a reset, take **STROBE** high if not already high, then force **DATA** low, and then take **STROBE** low again. After initiating the reset, while still holding **DATA** forced low, take **STROBE** high and then low again before releasing **DATA.** Then once again take **STROBE** high then low to complete the reset sequence. At the end of this sequence the ASIC will be in the very low-power "OFF" state. To arm the ASIC to read cards, one more sequence of taking **STROBE** high and then low is required. See TIMING AND CURRENT CONSUMPTION for the timing constraints applicable throughout this document.

DATA is normally an output to the ASIC held high in its default state, but the pin is designed with a one-shot strong pull-up in combination with a constant weak current-source drive such that a micro-controller may reliably overpower or force it low as part of initiating a reset. Note that the micro-controller unit (MCU) or other device pin connected to the ASIC's **DATA** pin must be a low-leakage input, such as found in typical CMOS devices. Furthermore the user's pin must have the capability of driving the pin low. If minimizing current consumption while forcing **DATA** low is desired, the MCU pin should *not* include a pull-up. A common configuration conveniently meeting these constraints is the open-drain "Port 0" I/O pin from the popular "8051" series of MCUs.

In addition to the steady-state weak current-source drive, the **DATA** pin employs a strong pull-up drive for a short duration with each rising edge of **DATA** as driven by the ASIC. This transient drive is needed to ensure high data rates with a capacitive load. It is not necessary or even desirable that the MCU pin have the current sinking capability to overcome this short-duration strong-pull-up driver.

During a user-initiated reset sequence, some delays are necessary when using an MCU with an open-drain line on **DATA**. This is because the short-duration strong pull-up drive is not active during the reset sequence, and only the weak current-source drive is available to pull **DATA** high. If desired, the reset sequence can be hastened by employing an MCU pin with an active high drive for **DATA**. Note that this optional active high drive can only be enabled during the reset sequence, as **DATA** is normally an output of the ASIC.

STROBE is a Schmitt-triggered digital input to the ASIC. It is mainly used to extract data from the ASIC as described below.

From the Armed-to-Read state, once three flux transitions have been detected, the ASIC signals "Card-Present" by pulling **DATA** low. It then begins to store data from the card into its buffer. The controller should respond to the Card-Present indication by taking **STROBE** high. The ASIC will respond to this rising edge of **STROBE** by taking **DATA** high, clearing the Card-Present indication. The controller should then take **STROBE** low and wait for **DATA** to fall, indicating the Buffer-Ready state. This falling edge of **DATA** is the signal to a micro-controller that the card swipe has ended, and the on-chip memory of the ASIC contains data to be read. The data is extracted or read from the buffer memory by pulsing the

STROBE input high and then low to advance the data pointer that steers the data to the **DATA** pin. During data extraction and when the **STROBE** input is low, a low on **DATA** represents a "one" bit and a high represents a "zero" bit. **DATA** returns to its default high state after each *rising* edge of the controller-issued **STROBE**. Note that after **DATA** initially falls to its Buffer-Ready state, the ASIC will ignore further card signals until reset.

The on-chip buffer (memory) is fixed at a size of 704 bits for each of the three magnetic stripe tracks—2112 bits total. The storage of each track begins with the first "one-bit" obtained from the card. The zero-bits that precede the first one-bit will not be stored. After detecting the first one-bit, the ASIC stores up to 704 bits per track; any bits exceeding this amount will be lost. This buffer size is more than adequate for ISO encoded cards.

Note that some damaged cards may have one or more initial zero-bits with media scratches that may appear as one-bits. The 704 bit buffer is large enough to even start storing data with a spurious one-bit at the very beginning of the card and still store out to the very end of the card for a data density of 210 bits per inch (bpi). For a robust system, firmware must anticipate these spurious one-bits and filter them appropriately. Also note that in the case of a backwards swipe, the ISO Longitudinal Redundancy Check (LRC) may have trailing zero-bits that are not stored in the chip's buffer. These missing bits are easily reconstructed with proper firmware. With the leading and trailing zero-bits characteristic of real-world magnetic stripe cards, it is impossible for any magnetic stripe decoder to reliably determine if particular leading/trailing zero-bits were intended as a part of the data, or are merely part of the synchronization zero-bits. Thus data storage begins with the first one-bit encountered.

Prior to issuing track 'A' data for the first time following a card swipe, the ASIC issues a "preamble" of 16 bits. This preamble indicates the revision of the ASIC. For this particular revision of the ASIC, it also indicates the mode. Note that package type is not reflected in the preamble. Respecting the same convention as for the actual card data, a low voltage level represents a "one" bit and a high voltage level represents a "zero" bit. The preamble is the first "data" issued following a card swipe, beginning with the first falling edge of **STROBE** after the Buffer-Ready indication, and is issued only once per data-extraction routine; it is not repeated until the chip has been reset, and another swipe is completed. A key to the preamble is shown below:

1100 0000 0000 0000 => MagTek Part Number 21006540/1 - New Mode

The Preamble is shown from right to left in the order it is transmitted. The first bit transmitted is the right-most bit shown.

Since the ASIC powers up in Old Mode by default, a power glitch or "brown-out" below the operating range of the ASIC (but perhaps not to the controller) could put the ASIC into Old Mode accidentally. If so, then the anticipated Buffer-Ready signal (per the New Mode protocol) will never be seen after the first falling edge of **STROBE**. In applications where it is possible for the ASIC to experience a "brown-out" without the controller's knowledge, a timeout of 1.7 seconds[2] should be used starting from this first falling edge of **STROBE**. If the timeout expires, then the ASIC is in Old Mode, and the controller can just reset the ASIC to remedy the situation, although any data will be lost.

[2] This timeout is obtained simply by dividing the maximum card length by the minimum card speed desired. For an ISO credit card at 5 cm/s, this timeout is about 1.7s. Shorter timeouts may be used if the minimum speed required is greater.

Alternatively, the controller can extract the data using the Old Mode protocol if desired. A reset must be actively issued to put the ASIC back into New Mode. The Old Mode reset resulting from the 14,610th rising edge of **STROBE** will leave the ASIC still in Old Mode. See OPERATION – OLD MODE and TIMING AND CURRENT CONSUMPTION.

Extraction of the data, as initiated by **STROBE**, proceeds in the order it was received for track 'A', 'B', and then 'C'. When the data pointer reaches the last position of the 2112 bit/3-track memory, it cycles back through the data in opposite order. To clarify, the data is shifted out first in the order it was received for track 'A' 'B' and then track 'C'. The ASIC does not determine the direction of the card swipe, but simply reports the data as it was received. Next, the opposite direction data shift-out also occurs in the order of track 'C', 'B', and then 'A', as if an audio or video tape were being "rewound". This process of data output in alternating order can occur indefinitely provided the ASIC is not reset.

To identify which track is providing data, the controller must count the issued strobes. If fewer than three tracks are implemented, the "empty" tracks, in addition to the preamble must still be extracted to reach the desired data.

The alternating data retrieval direction allows for the reading of cards swiped in either direction without using micro-controller memory to store all the card data. For both directions of card swipe, the card data can be verified for integrity before transmission to the host.

Initiating a reset clears the data buffer in the ASIC, setting the data therein to all 'zeroes' (high level). A reset may be performed at any time except within an already initiated reset routine. If an attempt at reset is made while a reset is still in progress (Trst_int not yet expired), then undefined operation may result. The ASIC will rearm to read quickly after a reset. If the ASIC should happen to rearm while a card swipe in progress, a partial swipe may be reported, although the report may be erroneous in cases where an adequate number of leading zero-bits was not available for synchronization.

NOTE THAT THE ASIC (IN ANY MODE) WILL RETAIN DATA INDEFINITELY UNTIL RESET. This is a convenience in many applications; however, MagTek recommends that care be exercised in minimizing the risk that sensitive data will be compromised.

The ASIC features circuitry that filters most ambient noise and prevents "bothering" the controller needlessly when there has been no card swipe. The signal from the magnetic head must first meet certain amplitude and frequency characteristics before any data is stored in the buffer. The ASIC must be able to establish a sufficiently stable bit-cell time-base from an adequate number of consecutive zero-bits before decoding can proceed. An absolute minimum of two leading zero-bits is required. Most cards can be read with as few as three leading zero-bits.

OPERATION – OLD MODE

Old Mode offers backwards compatibility with many designs using MagTek's 21006536/37 and 21006529/39 ASICs. Old Mode is not recommended for new designs.

To operate in Old Mode, it is only necessary to never *force* **DATA** low. The ASIC will always default to Old Mode when **DATA** is high as the ASIC enters its reset routine. Care should be taken to ensure this is the case during power-up. If New Mode is entered, it is impossible to revert back to Old Mode without cycling power to the chip. Only the differences between Old Mode and New Mode will be given below.

The shift-out buffer length in Old Mode is limited to 608 bits per track instead of 704 bits per track for New Mode.

There is no Card-Present indicator in Old Mode. A single falling edge of **DATA** is used for the Buffer-Ready signal following the completion of the card swipe.

STROBE is held high in the Armed-to-Read state instead of low.

A key to the Preamble for Old Mode is shown below. Note that the Preamble cannot be used to differentiate Old Mode from New Mode, since the protocol for extracting the Preamble differs between the two modes. See OPERATION – NEW MODE for details.

0100 0000 0000 0000 => MagTek Part Number 21006540/1 - Old Mode

The Preamble is shown from right to left in the order it is transmitted. The first bit transmitted is the right-most bit shown.

In Old Mode the process of data output in alternating order is limited to a maximum of four (4) forward-and-back cycles (total path = ABCCBAABCCBAABCCBAABCCBA) instead of unlimited cycling as is the case in New Mode.

The OFF state is not an available option in Old Mode. Note that "Sleep" as defined in the MagTek Specification 99875259 for the 21006536/37 and 99875336 for the 21006529/39 ASICs is equivalent to "Armed-to-Read" in this specification, and is, of course, available.

With Old Mode, there is only one method of initiating a reset to the ASIC other than cycling power. This is to issue all **STROBE** pulses required for the "ABCCBAABCCBAABCCBAABCCBA" data extraction sequence. Counting from first **STROBE** pulse (falling then rising edge) issued upon indication of the Buffer-Ready state, there are a total of 2+16+8*3*608= 14,610 **STROBE** pulses required to initiate the reset. After the 14,610th rising edge of **STROBE**, **DATA** will be taken to a high state as usual, and a reset will be initiated.

NOTE THAT THE ASIC (IN ANY MODE) WILL RETAIN DATA INDEFINITELY UNTIL RESET. This is a convenience in many applications; however, MagTek recommends that care be exercised in minimizing the risk that sensitive data will be compromised.

See MagTek Specification 99875259 for the 21006536/37 and 99875336 for the 21006529/39 ASICs for further details.

TIMING AND CURRENT CONSUMPTION

The signal timing and current consumption relationships are shown in Figures 1-5 below. The variations shown are strictly due to reset technique and mode. User constraints are shown in ***green***, and ASIC delays are shown in ***black***. For users without access to a color copy, the constraints and delays are separated below in the descriptions. "HS" indicates "Handshake". "CP" indicates "Card-Present". "BR" indicates "Buffer-Ready". The timing diagrams are not to scale.

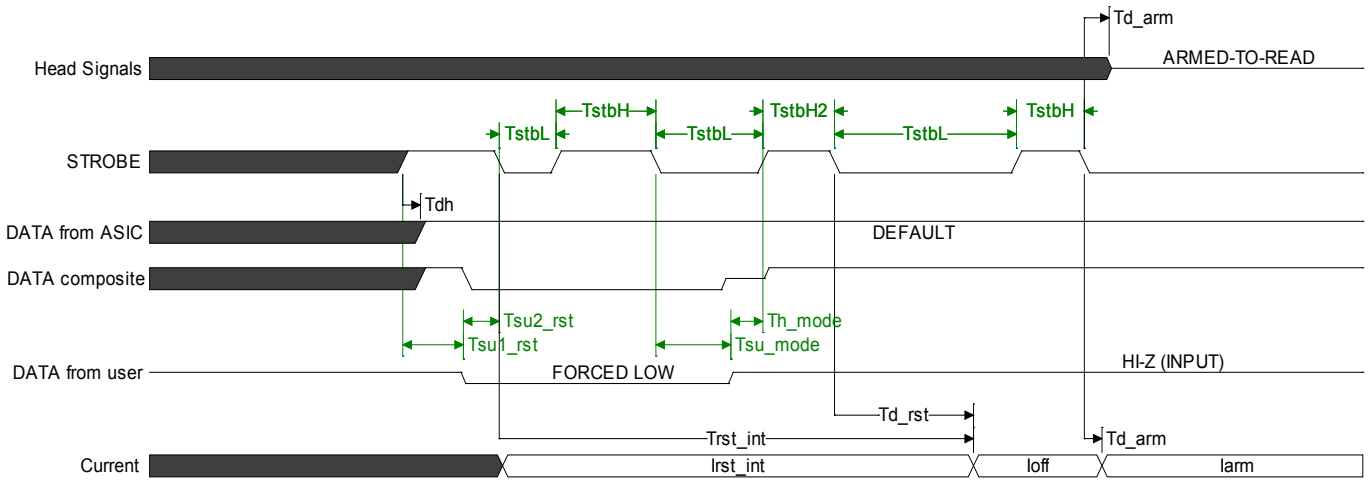


Figure 1. Timing and Current Consumption – New Mode Reset and Armed-to-Read Sequence Only; Showing the OFF State

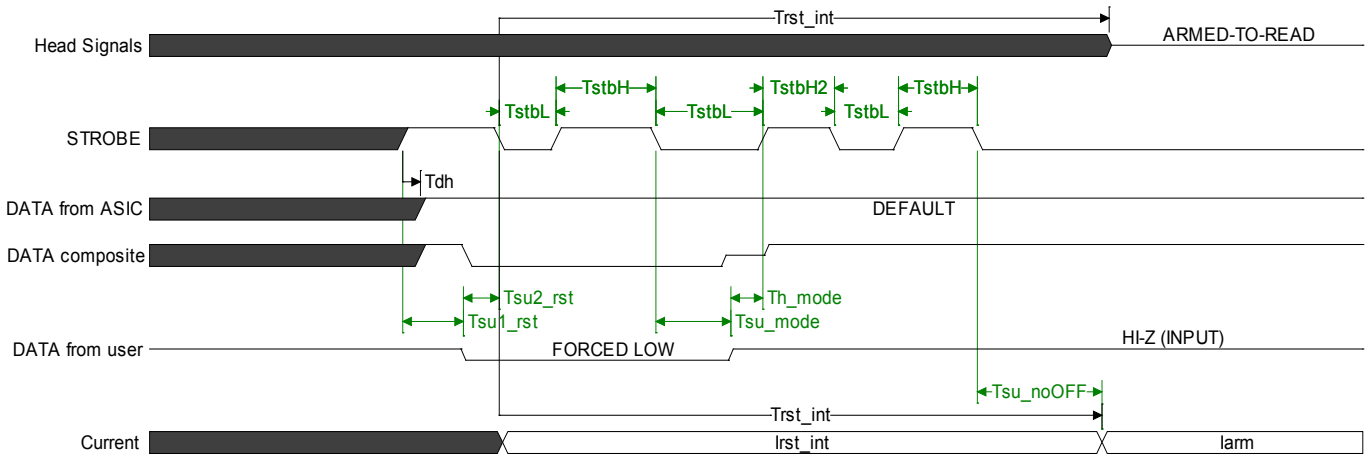


Figure 2. Timing and Current Consumption – New Mode Reset and Armed-to-Read Sequence Only; Showing the OFF State Skipped

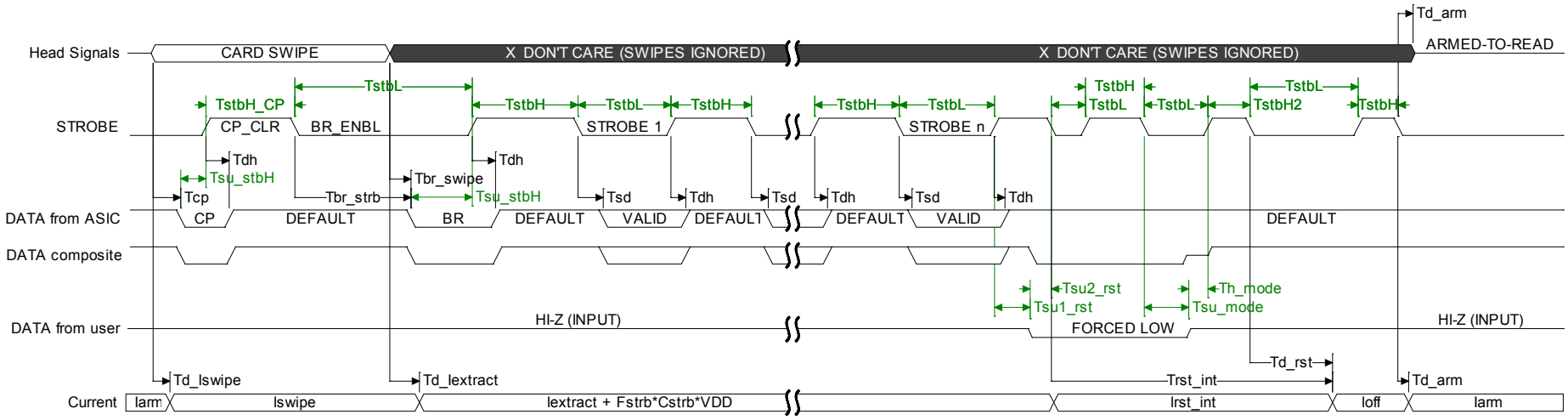


Figure 3. Timing and Current Consumption – Complete Sequence of Events from the Armed-to-Read State and Back Again; Showing a Quick Response to Card-Present; Showing the OFF State

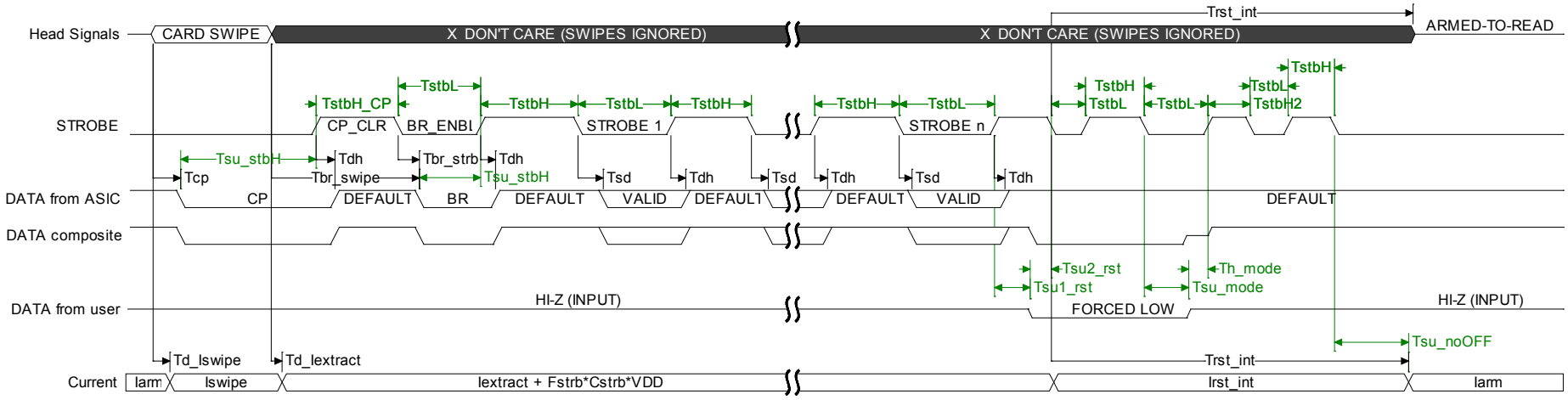


Figure 4. Timing and Current Consumption – Complete Sequence of Events from the Armed-to-Read State and Back Again; Showing a Slow Response to Card-Present; Showing the OFF State Skipped

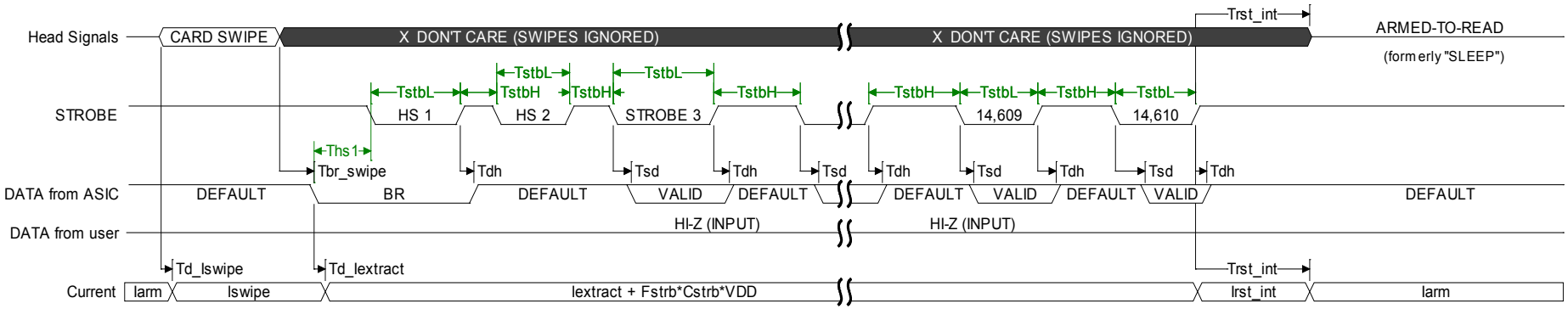


Figure 5. Timing and Current Consumption – Old Mode with 14,610 STROBE Reset (No OFF State in Old Mode); Complete Sequence of Events from the Armed-to-Read State and Back Again

Current Consumption

Iarm = 120 μA maximum

Iswipe = 1 mA maximum (internal oscillator running)

Iextract = 20 μA maximum for New Mode; 185 μA maximum for Old Mode

Cstrb = [1 nF maximum + parasitic capacitance of PCB] (this is the total capacitance driven by **STROBE** and its effects; sometimes called power-dissipation-capacitance)

Fstrb = User-controlled frequency of **STROBE** during data extraction

IdataLow = 48 μA maximum

Irst_int = 1 mA maximum (internal oscillator running; subtract ***IdataLow*** if **DATA** is released before ***Irst_int*** expires)

Ioff = 10 μA maximum

Example calculation for current consumption during New Mode data extraction:

Maximum parasitic PCB capacitance on **STROBE** (example) = 20 pF
Cstrb = 1 nF + 20pF
Fstrb = 1MHz
VDD = 3.3 V
Imax = ***Iextract*** + ***Fstrb*** * ***Cstrb*** * **VDD**
Imax = (20 μA) + (1 MHz) * (1020 pF) * (3.6 V)
Imax = 3.7 mA

A transient current of 1mA maximum, not shown in timing diagrams, may exist for the duration of ***Td_arm*** (Figures 1 and 3 only).

Timing – User Constraints

TstbL (**STROBE** low) = 250 ns minimum

Minimum allowable **STROBE** width (active-low).

TstbH (**STROBE** high) = 250 ns minimum

Minimum allowable **STROBE** high width (STROBE is active-low).

TstbH2 (**STROBE** high special case) = sufficient time to allow **DATA** to charge up to 0.85*V_{DD} prior to **STROBE** falling, given I_{OH_DATA} minimum (+ any current provided optionally by the MCU) and any capacitance on **DATA,** OR 250 ns, whichever is greater. Example: For a 50 pF capacitance on **DATA**, VDD at 3.6 V, I_{OH_DATA} minimum of 12 µA, and no MCU "assist", *TstbH2* can be no less than (50 pF)(0.85)(3.6 V)/(12 µA) = 12.75 µs.

Minimum allowable **STROBE** high width for the high-going **STROBE** pulse immediately following ***Th_mode*** (**STROBE** is active-low).

Tsu1_rst (Setup1 for reset) = 170 ns minimum

Recommended, but not required setup-time from the rising edge of **STROBE** to the falling edge of **DATA** as forced low by the user as part of initiating a reset. This is the time interval that the strong pull-up of **DATA** may be active. Thus **DATA** line contention during this time is best avoided to reduce the occurrence of current spikes.

Tsu2_rst (Setup2 for reset) = 4.5 µs minimum

Setup-time required from the falling edge of **DATA** as forced low by the user to the falling edge of **STROBE** used to initiate a reset.

Tsu_mode (Setup for Mode) = 20 ns minimum

Setup-time required from the falling edge of **STROBE** to the release of **DATA** (previously forced low by the user to initiate a reset). The term "mode" here refers to manufacturing test modes undefined to the user.

Th_mode (Hold for Mode) = 20 ns minimum

Hold-time required from the release of **DATA** (previously forced low by the user to initiate a reset) until **STROBE** is taken high. The term "mode" here refers to manufacturing test modes undefined to the user.

Tsu_stbH (Setup for taking **STROBE** high) = 20 ns minimum

Setup-time required from the falling edge of **DATA** in the case of indicating Buffer-Ready or Card-Present until the rising edge of **STROBE**.

TstbH_CP (**STROBE** high for Card-Present clear) = 1.1 µs minimum

Minimum allowable STROBE high width for the special case of clearing Card Present.

Tsu_noOFF (Setup required for no OFF state) = 20ns minimum

Setup-time required from the falling edge of **STROBE** that preemptively sets the Armed-to-Read state, to the expiration of Trst_int. This setup time is intended as an aid to understanding the operation of the chip and is normally of no concern to the user.

Whether or not the chip goes into the OFF state between reset and the Armed-to-Read state just depends upon how quickly the required **STROBE** pulses can be issued relative to Trst_int.

Ths1 (Handshake #1) = 20 ns minimum; Applicable only to Old Mode

Minimum time required from the initial falling edge of **DATA** before the first **STROBE** falling edge can be issued.

DATA extraction rate = 1 / (***TstbL_min***+***TstbL_max***) = 2 Mbits/sec maximum

Maximum **STROBE** rate when it is *not* required that the **DATA** line be readable = 10MHz (not shown in diagrams)

Old Mode Only - Strobing at this limit is useful for reducing the time required to reset the chip in Old Mode. New Mode users can reset the ASIC more easily by using **DATA** and **STROBE**.

Timing – ASIC Delays

Tcp (Card-Present) = any delay due to the wake-up mechanism (depends on card speed, encoding, amplitude, etc.). The first flux variation on HEAD_A/B/C of a negative polarity relative to the HEAD_COMMON pin to trip the wake-up threshold will activate wake-up. The third flux reversal from and including wake-up will activate Card-Present.

Tbr_swipe (Buffer-Ready due to swipe) = 35 ms maximum

Assuming as shown in Figure 3, that both a rising edge (CP_CLR) and a falling edge (BR_ENBL) of **STROBE** have been issued prior to the end of the card swipe:

Time from either the last flux reversal or from when the buffer becomes full for the last awakened track (whichever comes first) to the falling edge of **DATA** indicating Buffer-Ready.

Tbr_strb (Buffer-Ready due to **STROBE**) = 2 µs maximum

Assuming as shown in Figure 4, that the falling edge of **STROBE** used for BR_ENBL is *not* issued until well after (by at least ***Tbr_swipe***) the end of the card swipe:

Time from the falling edge of **STROBE** used for BR_ENBL, to the falling edge of **DATA** indicating Buffer-Ready.

Td_Iswipe (Delay for Swipe current) = 100 µs maximum

Time needed from the first detected flux reversal for the ASIC to transition from Iarm to Iswipe.

Td_Iextract (Delay for Extract current) = 10 µs maximum

Time needed from Buffer-Ready for the ASIC to transition from Iswipe to Iextract.

Tdh (**DATA** Hold) = 5 ns minimum

Time from rising edge of **STROBE** that **DATA** is still valid (or time from rising edge of **STROBE** until an attempt is begun to drive **DATA** high by the ASIC).

Tsd (**STROBE** to **DATA**) = 170 ns maximum

Time from falling edge of **STROBE** until **DATA** is valid.

Trst_int+ (Reset internal plus) = User-controlled time between the falling edge of **STROBE** used to generate a reset and the subsequent falling edge of **STROBE**. This time period is used in the calculation of the maximum ***Trst_int*** below.

Trst_int (Reset internal) = 3 ms minimum; [7.5 ms + ***"Trst_int+"***] maximum from a falling-**STROBE**-initiated reset.

New Mode: Delay from the initiation of reset to the end of the ASIC's internal reset in the case where **DATA** has been released and a rising then falling edge of **STROBE** provided prior to the expiration of this delay. The internal reset may be extended even beyond the above indicated maximum by delaying the falling edge of **STROBE** following the release of **DATA** (and a subsequent rising **STROBE** edge). See ***Td_rst***.

Old Mode: Delay from the initiation of reset to the end of the ASIC's internal reset. (Set ***"Trst_int+"*** to zero.)

Td_rst (Delay for end of Reset) = 2 µs maximum

Delay from the falling edge of **STROBE** following the release of **DATA** (and a subsequent rising **STROBE** edge) until the ASIC's internal reset ends. This delay applies only in the case where **DATA** has *not* been released and a rising then falling edge of **STROBE** provided prior to the expiration of ***Trst_int***. Upon the end of the internal reset, the ASIC transitions from a current consumption of ***Irst_int*** to one of ***Irst_off*** or ***Iarm***. Delaying this falling edge of **STROBE** beyond the expiration of ***Trst_int*** will cause the current consumption of the ASIC to remain at ***Irst_int*** until the appropriate falling edge of **STROBE** is issued and ***Td_rst*** expires.

Td_arm (Delay for Arm) = 110 µs maximum (Figures 1 and 3 only)

Delay from the falling edge of **STROBE** during the OFF state until the ASIC is armed to read cards. A transient current of up to 1mA may exist during this delay time. In addition to this delay, there is up to 1ms of settling time required before the ASIC will wake up to the smallest of input signals per this specification.

Trdy (Ready) = 10 ms maximum (not shown)

Initialization time required after VDD becomes valid. Note that the state of **DATA** may be indeterminate during this time and, therefore, an appropriate delay should be considered after applying power. **STROBE** should be held high, and **DATA** should be held high or high-Z during ***Trdy***. Under no circumstances should a falling edge of **STROBE** be allowed during ***Trdy.***

RECOMMENDATIONS AND PRECAUTIONS FOR MECHANICAL DESIGN

Most magnetic stripe reading devices on the market today, including this one, operate as temporal decoding devices as opposed to spatial decoding devices. Temporal decoding describes the technique of estimating the relative distances between flux reversals in the magnetic media by measuring the *time* that has elapsed between the flux reversals passing the magnetic head gap during the swipe of a card. Spatial decoding is a technique that allows for directly discerning the actual distances between flux reversals on the card, but this to apply technique is relatively expensive. Temporal decoding relies on the assumption that the acceleration from bit-cell to bit-cell as a card is swiped is insignificant in terms of distinguishing one-bits from zero-bits. This applies to *all* temporal decoding devices.

It is critical for the mechanical designer to increase the probability that this assumption is valid. Thus for a robust magnetic stripe reader there can be no sudden accelerations in the card path while the head gap is in contact with the magnetic stripe. For hand-swipe readers here is a list of common problems related to this concern that should be avoided while the magnetic media is in contact with the head:

1) Burrs or bumps in the card slot.
2) Smart-Card connectors contacting the card.
3) Card "gates" or latches that are actuated by the card motion.
4) Electro-mechanical switches that are actuated by the card motion.
5) Poor ergonomics that cause the hand to bump into an obstacle during the swipe.
6) Poor head spring design that allows the head to oscillate back and forth when a card is presented at high speed.

For motorized card-drive devices, additional care must be taken. Here are some common additional problems:

1) Stepper motor induced jitter.
2) Gear cogging induced jitter.

In addition to keeping the card motion smooth, the mechanical design must also minimize azimuth and track location errors, allow for embossed cards, and keep the magnetic head in very close contact with the magnetic stripe. Common problems related to these constraints include:

1) Head bounce causing poor head-to-stripe contact when the card is presented at high speeds.
2) Too wide a card slot, allowing the card to tilt beyond the compliance of the head spring, resulting in poor head-to-stripe contact.
3) Too short a "lead-in" or poor swiping ergonomics causing azimuth errors for the typical user. This is usually motivated by a desire to make the overall reader very small.
4) For insert-withdrawal or "dip" readers: azimuth error as the card is first inserted or right as it leaves the slot in the case of withdrawal. Consider a deeper slot and/or a "floating" wear-plate that allows the head to follow the azimuth error of the card as it enters/exits.

TECHNICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Conditions (-40°C to +85°C unless otherwise stated)	Value	Units
V_{DD}	Steady-state	-0.3 to 4.0	V
STROBE Input Voltage	Steady-state	-0.3 to VDD+0.3	V
STROBE Protection Diode Current	Steady-state	-20 to 20	mA
DATA Input Voltage	Steady-state	-0.3 to VDD+0.3	V
DATA Protection Diode Current	Steady-state	-20 to 20	mA
DATA Output Current Sourcing	Steady-state	Internally limited	
DATA Output Current Sinking	Steady-state	20	mA
Storage Temperature	Steady-state	-55 to 150	˚C
ESD Immunity	Human Body Model, JESD22-A114-A, class 2	2000	V
ESD Immunity	Machine Model, JESD22-A115-A, class 2	200	V
ESD Immunity	Charge Device Model, ESD-STM5.3.1-1999, classification C3	500	V
Latch-up Immunity	85°C, EIA/JESD78	100	mA
MTBF	Based on Mil-217	3.2 E07	Hrs

Electrical Characteristics and Recommended Operating Conditions

Parameter	Conditions (-40°C to +85°C)	Value		Units
		Min	Max	
V_{DD} Operating		2.7	3.6	V
V_{DD} Time Constant	To guarantee proper reset functioning under all conditions; Rise-time = 2.2 * (Time Constant)†	6		μs
I_{DD} Operating	See "Timing and Current Consumption" section			
V_{OL} DATA	V_{DD} = 2.7 V; I_{OL} = 2 mA		0.40	V
I_{OH} DATA	V_{DATA} = 0 V to 0.85*V_{DD}; Steady-state	12	48	μA
V_{IH} DATA		0.80* V_{DD}		V
V_{IL} DATA			0.20* V_{DD}	V
VT+ STROBE	Positive-going threshold	0.40* V_{DD}	0.80* V_{DD}	V
VT- STROBE	Negative-going threshold	0.20* V_{DD}	0.40* V_{DD}	V
Hysteresis STROBE	VT+ - VT-	0.4	1.2	V
I_{IN} Leakage STROBE	V_{IN} = 0 V to V_{DD}	-10	+10	μA
C_{LOAD} HEAD_COMMON			50	pF
C_{LOAD} DATA‡			50	pF
Head Inductance*	@ 1kHz	25	250	mH
Head Sensitivity*	Pk-to-Pk amplitude; ISO 7811 100% reference	1.1	2.0	mV/cm/s
Head Resistance*	(DC)	0	500	Ω
Head Track Width	(the ASIC is optimized for a track width of no less than this; reduced performance may result from narrower track widths)	800		μm
Head Gap Length	(the ASIC is optimized for a gap length of no more than this; reduced performance may result from longer gap lengths)		35	μm
Resistance from HEAD_COMMON to GND ††	Measured at a 3V potential	10	-	MΩ
Resistance from HEAD_A/B/C to GND ††	Measured at a 3V potential	10	-	MΩ
Resistive load of Head ††	This load is varied as the chip operates. Additional loading must not be introduced.	0.50	85	kΩ

† A 10Ω and 1.0uF may be used to filter V_{DD} if necessary to meet the 6us minimum time-constant requirement. Both the capacitor and resistor are available in the "0402" size. Note that in New Mode this is not necessary since the user can perform a reset at any time (assuming V_{DD} is in the proper range at the time of reset).

‡ Exceeding CLOAD Max DATA will affect the maximum rate of DATA.

†† These specifications are provided to quantify how isolated the magnetic head must be in the event that contaminants, such as from soldering the head wires to the head, leave unwanted conductive paths between the various head pins and ground.

* Two heads may be used in parallel or in series as long as the inductance, resistance, and sensitivity ranges shown are respected. A slight reduction in performance may result.

PACKAGING AND DRAWINGS

Packaging and Pin Assignments

Signal and pin assignments for the Decode ASIC are shown in Table 1.

Table 1. Signal and Pin Assignments – Triple Track ASIC

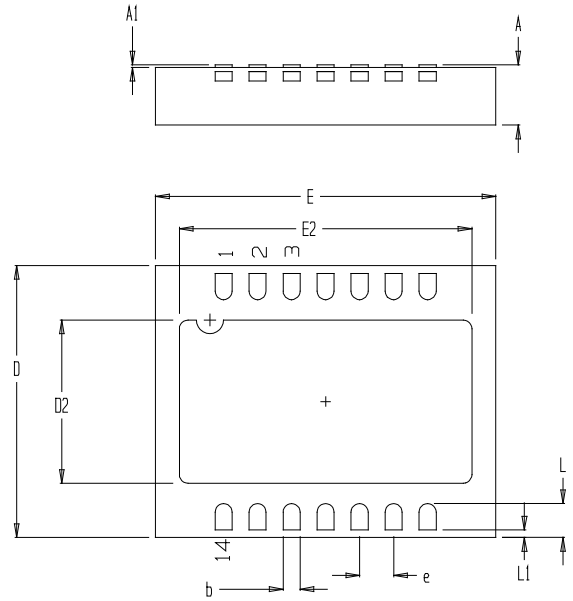
MLF14 Pin Number	Pin Name
1	HEAD_COMMON
2	NC
3	HEAD_A
4	NC
5	HEAD_B
6	NC
7	HEAD_C
8	STROBE
9	NC
10	DATA
11	NC
12	VSS
13	VDD
14	NC

A single 0.1uF decoupling capacitor is required. "NC" indicates "No Connection". These "NC" pins are not connected internally.

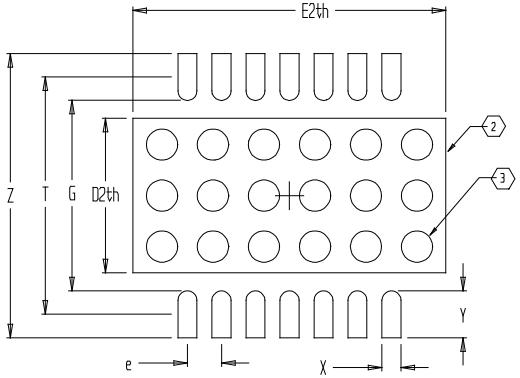
Mechanical Drawings

The 14 pin 4mm x 5 mm MLF™ (*Micro*LeadFrame™) package is shown in Figure 6. Package marking drawings are shown in Figures 7 and 8.

REVISIONS			
REV	DESCRIPTION	CHANGED BY	DATE
A	CHANGED NOTE 3 PER ECN 51395	RH	12JAN04



BOTTOM VIEW



RECOMMENDED PAD LAYOUT

TOP VIEW

SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.85	1.00
A1	0.00	0.01	0.05
A3		0.20 REF.	
b	0.20	0.25	0.30
e		0.50 BSC	
L	0.45	0.50	0.65
D		4.00 BSC	
E		5.00 BSC	
D2	2.25	2.40	2.55
E2	4.15	4.30	4.45
L1	-	-	.15
Z		4.180 BSC	
G		2.800 BSC	
X		0.280 BSC	
Y		0.690 BSC	
D2th		2.273 BSC	
E2th		4.600 BSC	
T		3.490 BSC	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMS ARE IN MM.
2. SOLID THERMAL PAD 100% VOID OF SOLDER MASK.
3. SOLDER PASTE:
   PERIMETER PADS TO BE 1:1 TO PCB LAND PADS.
   THERMAL PAD OPENING MUST GIVE 50 TO 80% COVERAGE.
   PATTERN SHOWN GIVES APPROXIMATELY 60% COVERAGE USING SOLDER PASTE DOTS 0.46 DIA ON 0.75 PITCH 18EA.
   TEMPLATE SHOULD BE LASER CUT AND ELECTRO POLISHED.
4. SOLDER MASK SHOULD BE CUT BACK 0.06 FROM ALL LAND PATERNS.
5. FOR MORE DETAILS SEE AMKOR'S
   APPLICATION NOTES FOR SURFACE MOUNT ASSEMBLY OF AMKOR'S MICROLEADFRAME (MLF) PACKAGES.

TOLERANCES:	X ±.05 XX ±.02 XXX ±.005 ANGLES ±1°
DRAWN BY	R. HOLMES
DATE	02DEC02
DESIGNER	R. HOLMES

MAGTEK 20725 S. ANNALEE AVENUE CARSON, CA 90746

MLF14 BASIC DIMS AND LAND PATTERN

SIZE	DWG NO.	REV
B	21006538	A
	SCALE FULL	SHEET 1 OF 1

Figure 6. 14 pin 4 mm x 5 mm MLF™ (MicroLeadFrame™)

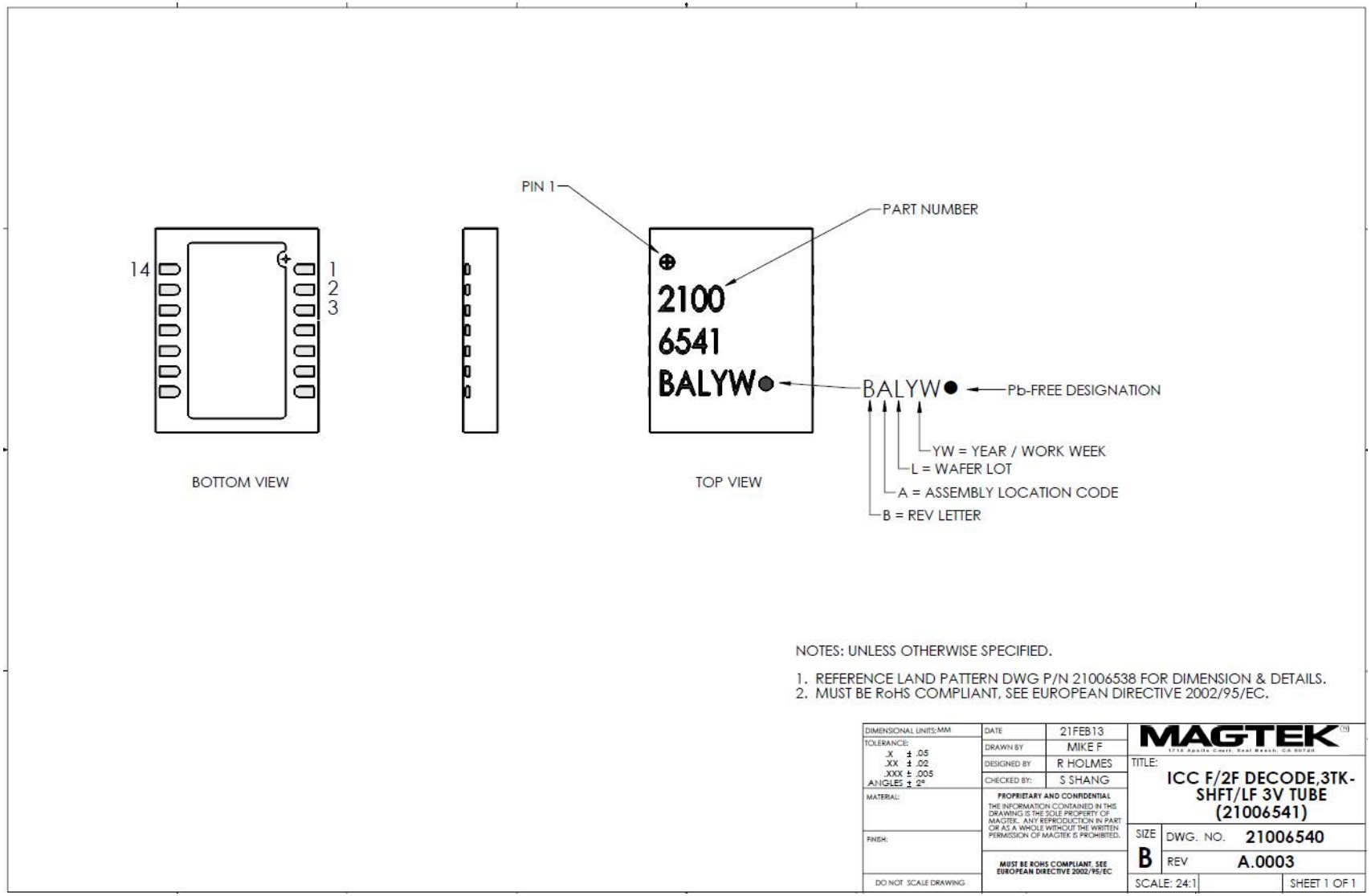


Figure 7. Package Marking for 21006540

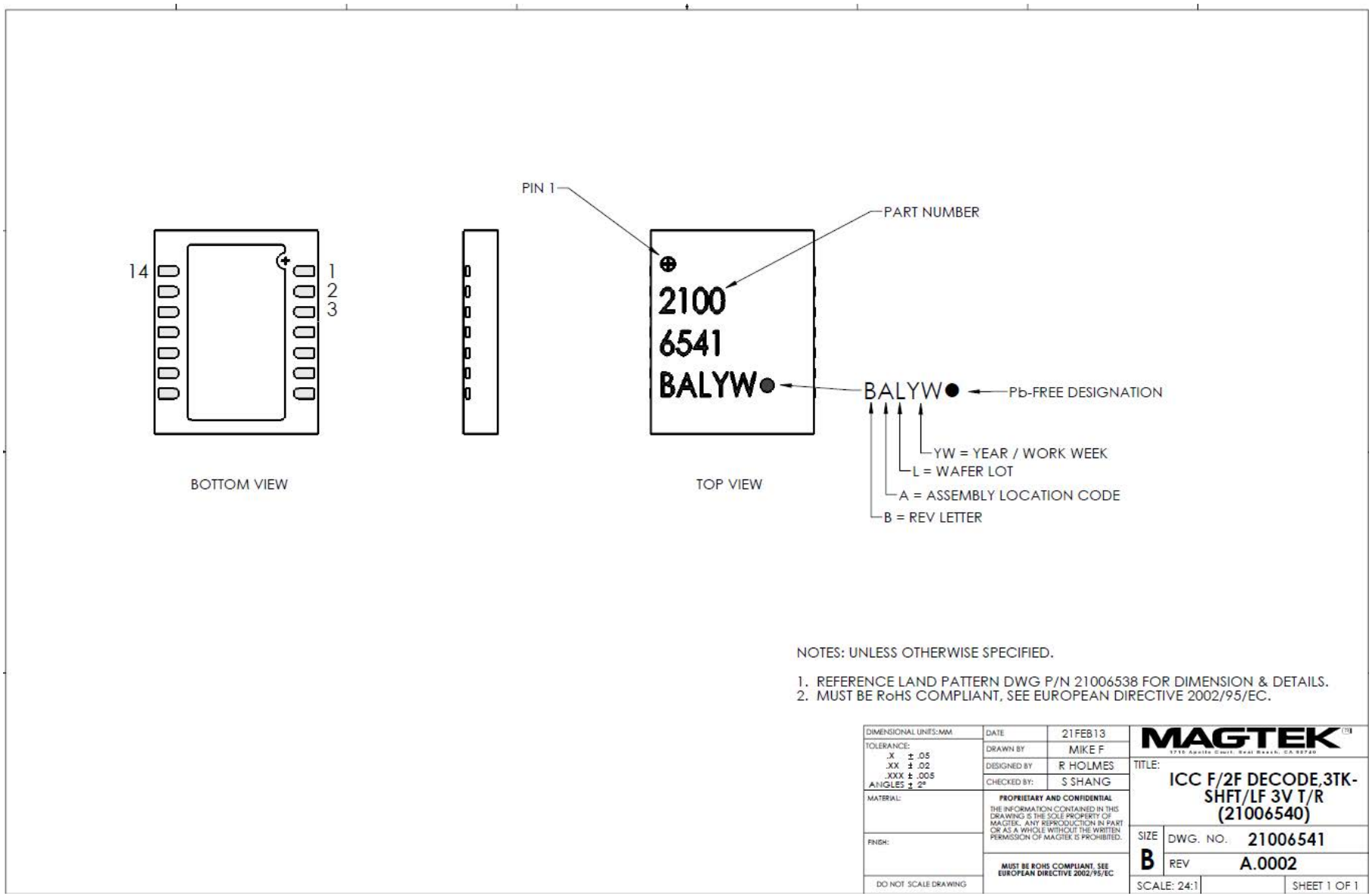


Figure 8. Package Marking for 21006541

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS AND SCHEMATICS

As with any analog or mixed-signal circuit, PCB layout must be approached with care to achieve optimal results with the Triple Track ASIC.

- The low-level analog head signals must be routed clear of any noise sources or digital signals. Use a quiet ground or other low impedance DC source to shield if necessary.
- The loop formed by each head signal conductor and its return path must be minimized to reduce noise pickup. Each track's pair of conductors must be routed with minimal clearance between them.
- The chip should be decoupled with a 0.1uF ceramic capacitor placed as close as possible to the DVDD and DVSS pins with minimal length traces connecting the cap to the chip, avoiding vias.
- DO NOT add additional head loading (resistance or capacitance) to the circuit. Head loading for this chip is dynamic, self-adjusting, and completely built into the chip. Additional head loading may degrade performance.
- Unused HEAD_A/B/C pins must not be connected to any potential. Leave these pins unconnected if unused.

The Triple Track ASIC is also available integrated into a magnetic head. As an alternative to a separate ASIC and magnetic head, the Shift-Out IntelliHead product can be easily accommodated on the PCB with very little if any additional board area. Shown in each of the recommended PCB layouts for the Triple Track ASIC is a "hook" for the Shift-Out IntelliHead in the form of a 5-pin connector. If using the Shift-Out IntelliHead, the only component that need be installed on the board is this 5 pin connector. If not using the Shift-Out IntelliHead, the 7-pin connector along with all the other components is installed instead of the 5 pin connector. The 7 pin and 5 pin connectors are mutually exclusive in terms of installation. MagTek recommends that this "hook" be included in all Triple Track ASIC PCB layouts so that the customer may have the option of using the Shift-Out IntelliHead with its performance benefits and possible future cost reduction benefits.

A note concerning Shift-Out IntelliHead compatibility: The on-chip memory tracks of the Shift-Out IntelliHead are permanently assigned to particular tracks of the magnetic head via internal wires connecting the head coil wires to particular inputs of the built-in ASIC. Typically the dual-track Shift-Out IntelliHead serves as a track 1&2 reader. As such, tracks 'A' and 'B' of the ASIC correspond to tracks '1' and '2' of the reader respectively when the Shift-Out IntelliHead/spring is mounted as designed, with the centerline of the spring mounting holes running through the center of track 2. For the less common track 2&3 reader, this Shift-Out IntelliHead/spring assembly may be used in an inverted configuration on the same chassis used by a track 1&2 reader. In this case, on-chip memory track 'A' corresponds to physical magnetic stripe track 3, and on-chip memory track 'B' corresponds to physical magnetic stripe track 2. This is important since it affects the arrangement of the data upon extraction from the chip. For the triple-track Shift-Out IntelliHead, tracks 'A', 'B', and 'C' of the ASIC are assigned to tracks '1', '2', and '3' respectively of the reader. MagTek recommends that these track assignments be respected when using the stand-alone chip to allow for easy migration to the Shift-Out IntelliHead products.

The 7-pin connector shown in all PCB layouts is Molex part number 53048-0710. The 5-pin connector shown in all PCB layouts is Molex part number 53048-0510. Other head connectors may be used of course, but these connectors ensure compatibility when using MagTek head assemblies.

The MLF™-14 is a near-chip-scale package, and requires some care for proper assembly. It is recommended, but not required, that the relatively large pad on the bottom of the package be grounded. For details concerning this package please visit http://www.amkor.com/Products/all_products/MLF.cfm

A recommended PCB land pattern for the MLF™-14 package is included in this section. MagTek has successfully used this land pattern in our manufacturing process, but cannot guarantee success in any situation, as manufacturing processes do vary. The MLF™ or similar package is also known as the QFN (Quad-Flat-No-lead) package.

For information on proper soldering techniques, refer to IPC/JEDEC J-STD-020C.

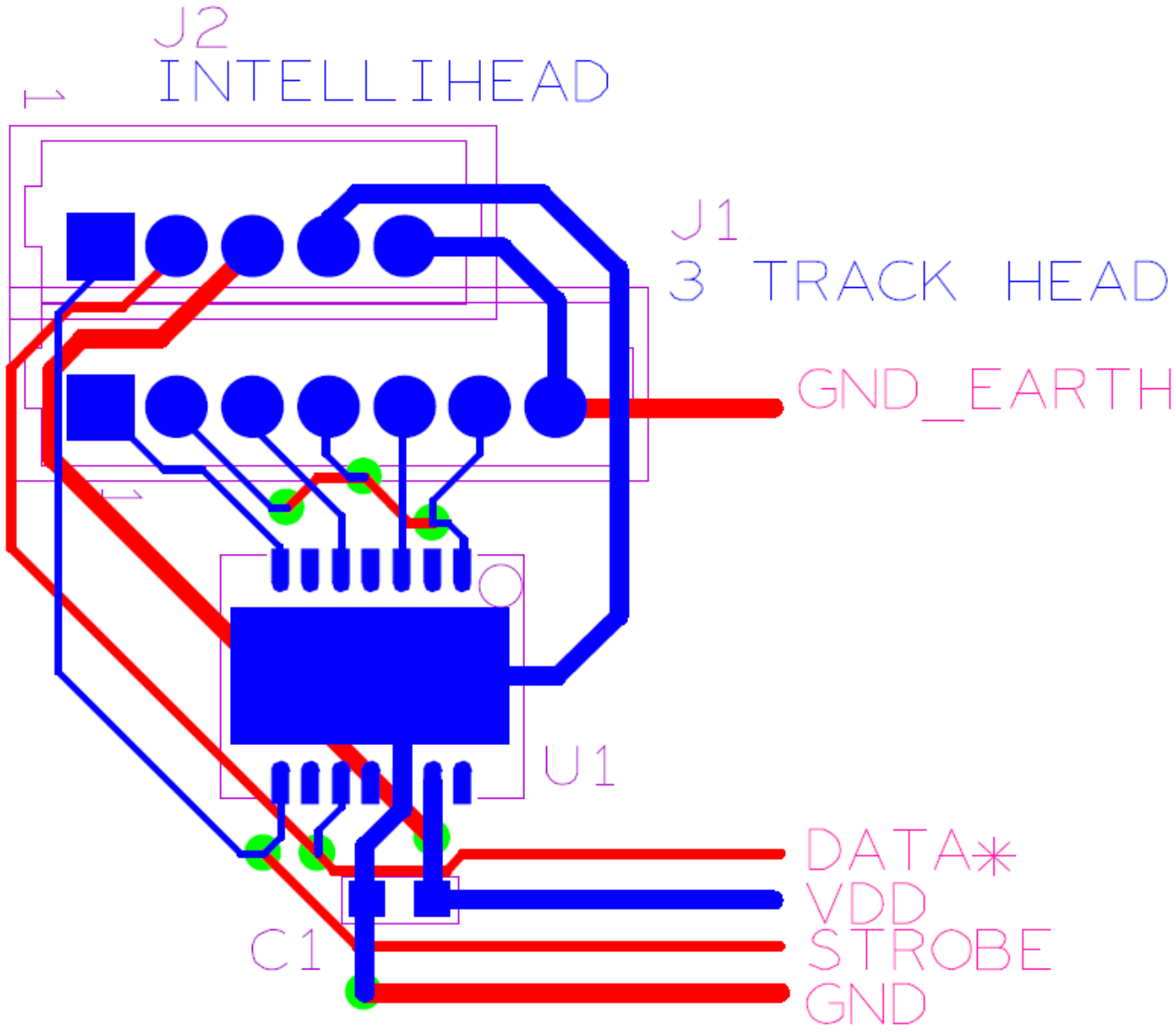
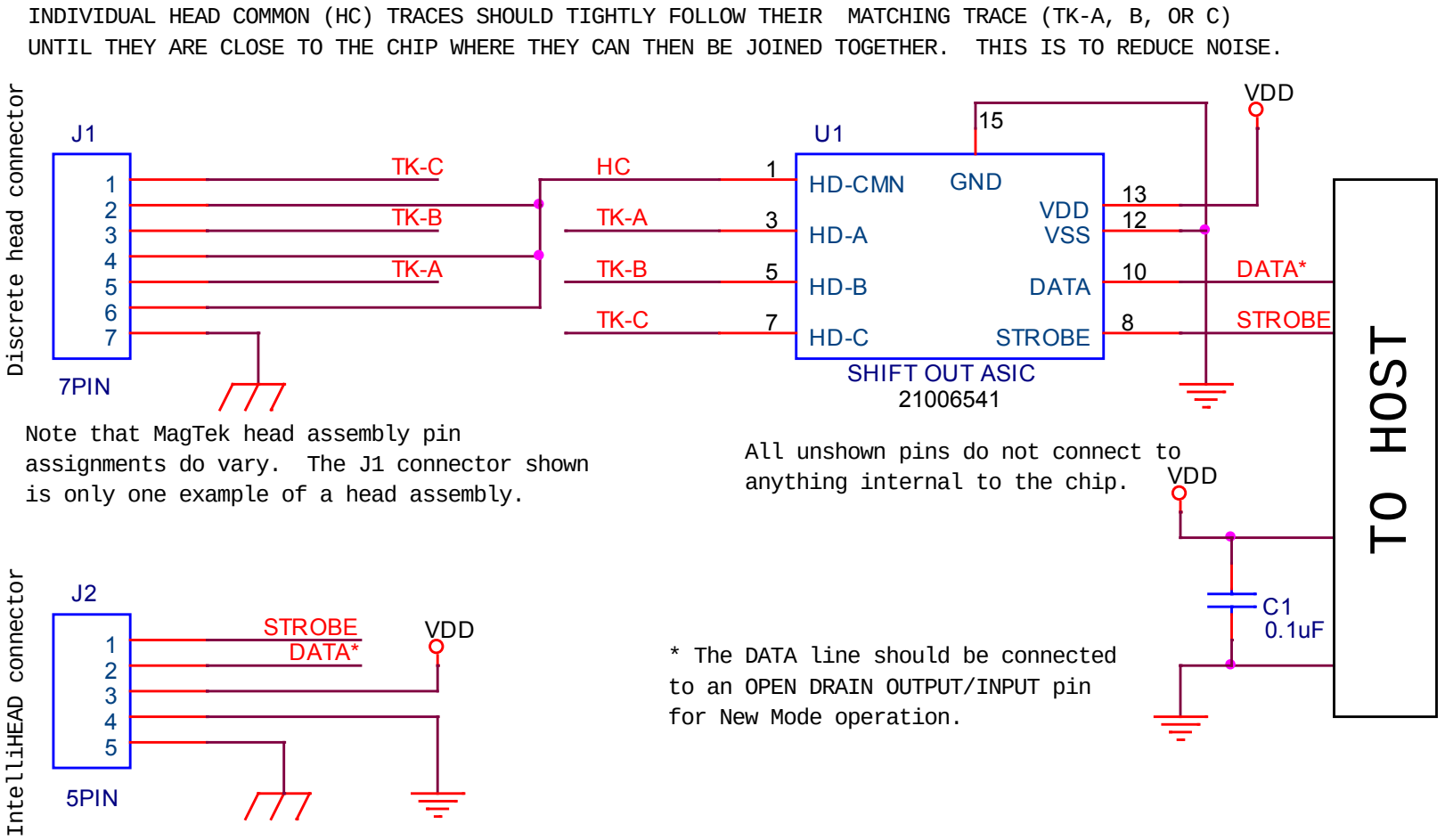


Figure 9. Example PCB Layout for MLF-14 with Provision for Shift-Out IntelliHead



Head case ground shown connected to earth ground via the head/IntelliHead connector. It is better to connect the head case ground directly to a separate earth ground if possible, bypassing the closely spaced PCB connector terminals. If this is not possible, as is the case in many designs, then the next best thing is to pass the earth ground through the board on its way to earth. Tying earth ground to signal ground on the PCB is often done, but problems can arise in the case of extreme ESD events.

Figure 10. Example PCB Schematic for MLF-14 with Provision for Shift-Out IntelliHead