SWIPE READERS
WITH 3-TRACK SPI INTELLIHEAD
TECHNICAL REFERENCE MANUAL

Manual Part Number 99875308-7

SEPTEMBER 2011

REVISIONS

Rev Number	Date	Notes
1	25 Oct 04	Initial Release
2	3 Jan 05	Appendix B: Replaced drawing 21044006A with 21044006B.
3	25 Jan 05	Sec 1, Table 1-1: Changed description of P/N 21044006 to Tracks 1,2,3 and Cable lengths to 90mm.
4	1 Feb 05	Editorial throughout. Sec 1: Updated Specifications, Table 1-2.
5	7 Mar 08	Added drawings 21030023, 21045096, 21047025.
6	10 Sept 09	Removed 21030023, 21045096, 21047025. Updated Limited Warranty & Agency Approvals
7	19 Sept 11	Added 21030023

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SECTION 1. FEATURES AND SPECIFICATIONS

The Swipe Readers with 3-Track SPI IntelliHead^{TM} provide magstripe reading capabilities for use in retail access control, time and attendance, and other applications.

The Reader chassis provides an industry standard mechanical footprint, along with magstripe head capabilities, which comply with ISO 7810 and AAMVA standards. The SPI (Serial Peripheral Interface) is a synchronous serial bus used for communication between the Reader and the target system.

MODELS

The current configuration is listed in Table 1-1.

Table 1-1. Models

Part Number	Description	Tracks	Cable Length	Appendix
21030023	90mm with SPI IntelliHead	1, 2, 3	140mm	B
21044006	43mm with SPI IntelliHead	1, 2, 3	90mm	B

FEATURES

- SPI bus compatible 3 wire serial interface. Supports SPI Mode A (CPOL = 1, CPHA = 1) and Mode D (CPOL = 0, CPHA = 0)

- Maximum SPI bus transfer rate of 100 Kbits/Second

- Reads card in both forward and reverse swipe directions

- Reads 1 to 3 tracks of encoded data meeting ISO 7810, 7811 standards

- Reads track 3 data encoded to ISO 4909 or AAMVA (Drivers license/ID Card) standards

- Less than 1 mA in standby mode

SPECIFICATIONS

The specifications are listed in Table 1-2 and in the appendices where noted.

Table 1-2. Specifications

STANDARDS	
Card Reading	ISO and AAMVA*
Flammability	Meets UL94V-0
Speed	Card speed through the unit may vary from: 3 to 60 in/s (7.6 to 152.4 cm/s)

ELECTRICAL		
All specifications below apply for Vin = +4 VDC to +15 VDC over the operational temperature range of –40 ^{o}C to +70 ^{o}C. See Figure 3-1 for timing diagram.		
Reader Idle Current:	< 0.9 mA typical at +25 ^{o}C	
Card Swipe Current:	9 mA typical at +25 ^{o}C	
Reader Idle Current:	< 1 mA typical over operational temperature range	
Card Swipe Current:	12 mA typical over operational temperature range	
SCL Input Signal:	Input High Voltage: Input Low Voltage:	2.0 V min, 5.0 V max 0.8 V max
SDA and DAV Output Signals:	Output High Voltage: Output Low Voltage:	2.6 V min at I_{OH} = - 3 mA 3.2 V min at I_{OH} = - 10 uA 2.5 V typ at I_{OH} = - 10 mA 0.6 V max at I_{OL} = 8.5 mA 0.1 V max at I_{OL} = 10 uA 1.0 V typ at I_{OL} = 25 mA

MECHANICAL	
Dimensions	See appendix relative to product
Connectors	See appendix relative to product
Life	1,000,000 passes

ENVIRONMENTAL	
Temperature	
Operating:	-40 ^{o}C to +70 ^{o}C (-40 ^{o}F to +158 ^{o}F)
Storage:	-40 ^{o}C to +70 ^{o}C (-40 ^{o}F to +158 ^{o}F)
Humidity	
Operating:	10% to 90% noncondensing
Storage:	10% to 90% noncondensing
Altitude	
Operating:	0-10,000 ft. (0-3048m)
Storage:	0-50,000 ft. (0-15,240m)

* ISO (International Standards Organization) and AAMVA (American Association of Motor Vehicle Administrators)

SECTION 2. INSTALLATION

This section consists of installation and connection of the Reader.

MOUNTING

The dimensions for mounting are shown in Appendix B.

MATING CONNECTOR

The mating connector for the SPI IntelliHead Reader is

> JST P/N B5B-ZR or S5B-ZR

INTERFACE

Interface connections are shown in Appendix B.

SECTION 3. OPERATION

This section describes the SPI (Serial Peripheral Interface), the SPI bus interface timing, power up messages and timeouts, card data transmission timeouts, and data output format. For a description of abbreviations see Table 3-1 and Figure 3-1 below.

Table 3-1. Description of Terms

Term	Description
DAV	Data Valid (output)
CPHA	Clock Phase
CPOL	Clock Polarity
LSB	Least Significant Bit
MSB	Most Significant Bit
SCL	Serial Clock (input)
SDA	Serial Data (output)
SPI	Serial Peripheral Interface

SPI

The SPI interface can be thought of as a variable-byte parallel to serial shift register. A variable number of data bytes are transmitted serially in 8-bit groups in the order of MSB to LSB. Data transfers occur when the DAV (Data Valid) status line is high.

For example, the bit transmission order for consecutive bytes A and B would be:

A(bit 7) A(bit 6) … A(bit 0) B(bit 7) B(bit 6) … B(bit 0)

Referring to Figure 3-1, the first data bit (MSB of the first byte to transmit) is set up prior to DAV assertion. DAV is raised high by the reader and data on the SDA line is then clocked out by the Host via the SCL line.

Data can be clocked into the Host on the rising edge of SCL or the Host can sample SDA while the SCL clock line is high. When the SCL clock goes low, the reader will fetch the next bit to place onto the SDA line.

After the last bit (LSB) of the last data byte is received by the Host, the reader will wait for the Host to lower SCL. When SCL is returned low, the reader will set DAV low to indicate that all data has been transmitted. The reader will remain in an idle state (with reduced current draw) until a new card swipe occurs. The DAV line will then be reasserted when the reader has collected the card data and is ready to transmit it to the Host.

Two SPI modes are supported by this reader, Mode A (CPHA=1, CPOL=1) and Mode D (CPHA=0, CPOL=0). Mode A means that the SCL clock line idles in a high state prior to DAV assertion. For Mode D, SCL idles low. Otherwise, data is collected by the Host in the same manner, either on the rising edge of SCL or while SCL is high.

The SPI Bus Interface Timing is shown in Figure 3-1.

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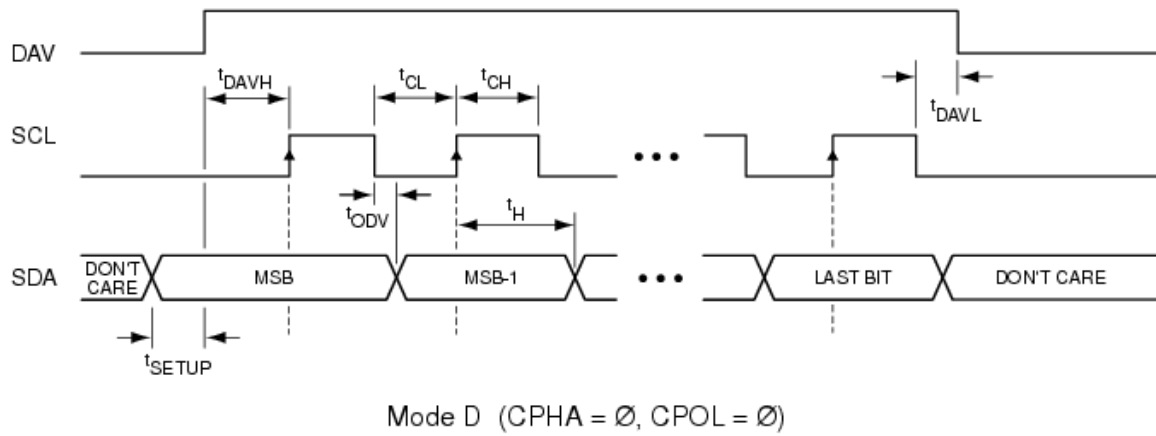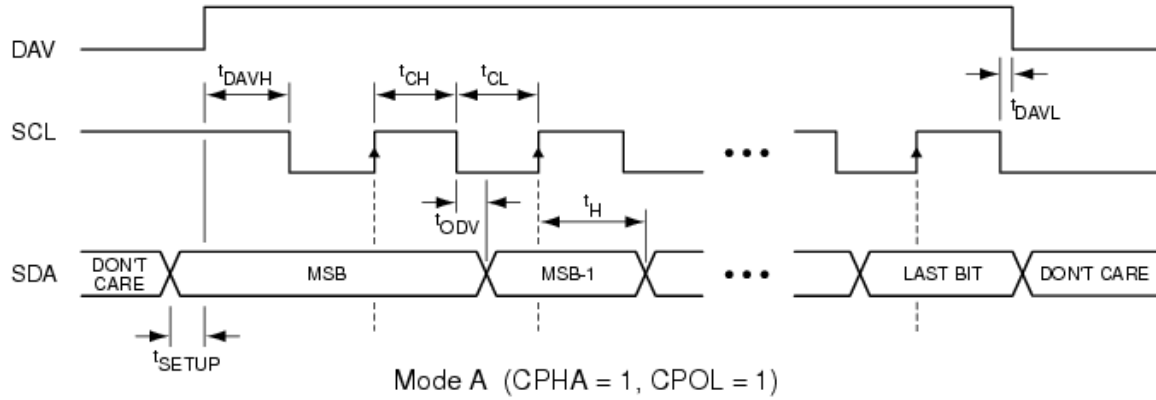
Symbol	Parameter	Minimum	Maximum
t_{CH}	Clock High Time	5 µs	100 mS
t_{CL}	Clock Low Time	5 µs	100 mS
t_H	Data Hold Time	t_{CH}	—
t_{DAVH}	DAV High to SCL Transition	Ø	400 mS
t_{ODV}	SCL Neg Edge to Output Data Valid	—	4.3 µs
t_{DAVL}	SCL Neg Edge to DAV Low	625 nS	8 µs
t_{SETUP}	Output Data Setup Prior to DAV High	83 nS	—

Figure 3-1. SPI Bus Interface TimingCard Data Transmission Timeouts

CARD DATA TRANSMISSION TIMEOUTS

The SPI bus timeouts, when card swipe data is available for transmission, are identical to that of the start up message. When card data is available, after a card swipe, the DAV line will be asserted high. The Host should respond (transition the SCL line) within 400 mS to prevent a timeout.

To collect all successive data bits, the Host should respond within 100 mS (i.e., should transition the SCL line at least once every 100 mS). This corresponds to a new bit collected every 200 mS for a minimum data rate of 5 bits/second. The maximum collection rate is 100 Kbits/second.

After the card data is transmitted, the reader will erase the card data from its memory and await a new card swipe. If a timeout occurs during transmission, the remainder of the card data will not be sent, the card data memory will be erased, and the reader will await a new card swipe.

DATA OUTPUT FORMAT

After a card swipe (forward or reverse), the data is transmitted in the following order:

<CR> <LF> [track 1 data] [track 2 data] [track 3 data] <00h>

Where:

<CR> is an ASCII carriage return (0Dh)

<LF> is an ASCII line feed (0Ah)

[track 1 data], if present, is comprised of a "%" start sentinel character, track 1 card data, and "?" end sentinel character.

[track 2 data], if present, is comprised of a ";" start sentinel character, track 2 card data, and "?" end sentinel character.

[track 3 data], if present, is comprised of a "+" start sentinel character, track 3 card data, and "?" end sentinel character.

<00h> is a binary zero termination character.

If any errors are detected in the card data, for a particular track, the reader will send an "E" for that track's card data. For example, if an error is detected in track 3 data, the reader will send +E? for [track 3 data].

Errors include: character parity error, track data LRC error, and start sentinel found but end sentinel missing.

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POWER UP MESSAGE AND TIMEOUTS

Between 10 to 15 milliseconds (mS) after power up, the reader will assert DAV to indicate that the start up message is ready to be sent over the SPI bus. This message is comprised of the text "SPI MAGTEK" followed by the firmware part number, an ASCII line feed (0Ah), and a binary zero (00h) termination character.

An example start up message appears below:

<div align="center">SPI MAGTEK 21088831C01<LF><00h></div>

If the Host does not respond to the DAV assertion between 400 to 600 mS (i.e. by transitioning the SCL line), the reader will time out and the start up message will not be sent. Thus, to prevent this timeout, the Host should respond within 400 mS after DAV is asserted high.

The timeout for successive data bits, in the start up message, is between 100 to 150 mS. To ensure a timeout does not occur, the Host should transition the SCL line at least once every 100 mS. This would correspond to collection of a new data bit every 200 mS for a minimum data rate of 5 bits/second. Data can be clocked out at a maximum rate of 100 Kbits/second.

If a timeout occurs, the remainder of the startup message will not be transmitted. After the start up message is transmitted (or not transmitted in the event of a timeout), the reader will then await a card swipe.

APPENDIX A. CODED CHARACTER SETS

The coded character sets are shown in the tables below.

Track 1 Coded Character Set (ISO)

Track 3 Coded Character Set (AAMVA)

Card Data	Serial Output	Card Data	Serial Output
0x00	Space	0x10	0
0x01	!	0x11	1
0x02	"	0x12	2
0x03	#	0x13	3
0x04	$	0x14	4
0x05	%	0x15	5
0x06	&	0x16	6
0x07	'	0x17	7
0x08	(	0x18	8
0x09	)	0x19	9
0x0A	*	0x1A	:
0x0B	+	0x1B	;
0x0C	,	0x1C	<
0x0D	-	0x1D	=
0x0E	.	0x1E	>
0x0F	/	0x1F	?

Card Data	Serial Output	Card Data	Serial Output
0x20	@	0x30	P
0x21	A	0x31	Q
0x22	B	0x32	R
0x23	C	0x33	S
0x24	D	0x34	T
0x25	E	0x35	U
0x26	F	0x36	V
0x27	G	0x37	W
0x28	H	0x38	X
0x29	I	0x39	Y
0x2A	J	0x3A	Z
0x2B	K	0x3B	[
0x2C	L	0x3C	\
0x2D	M	0x3D	]
0x2E	N	0x3E	^
0x2F	O	0x3F	_

Track 2 and 3 Coded Character Set (ISO)

Card Data	Serial Output
0x00	0
0x01	1
0x02	2
0x03	3
0x04	4
0x05	5
0x06	6
0x07	7
0x08	8
0x09	9
0x0A	Account Separator (:)
0x0B	Start Sentinel (;)
0x0C	<
0x0D	Field Separator (=)
0x0E	>
0x0F	End Sentinel (?)

APPENDIX B. DRAWINGS

The following drawing is provided in this section:

Part Number Title

21030023   3TK SPI IntelliHead, 90mm Swipe Reader, 140mm wire, 5PJST Connector

21044006   3TK SPI IntelliHead, 43mm Swipe Reader, 140mm wire, 5PJST Connector

ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	21030504	APC PCB ASSY,3TK SPI INTHD	1
2	21030902	REF TEST SUPPORT KIT,SPI INTHD	1
3	21052805	PSY 3TK 7MM HD (S) W/SPRING FOR INTHD,NO PINS	1
4	70832015	WRE WIRE 32AWG,7-STRAND WHITE	.48
5	70832025	WRE WIRE 32AWG,7-STRAND BLACK	.48
6	70832035	WRE WIRE 32AWG,7-STRAND GREEN	.48
7	70832055	WRE WIRE 32AWG,7-STRAND YELLOW	.48
8	70832085	WRE WIRE 32AWG,7-STRAND RED	.48
9	78400221	CON CONN 5PIN FEM,JST ZHR-5	1
10	81900073	TML TERMINAL CRIMP #28-32AWG (REEL)-JST	5
11	94100127	LBL REF LABEL,GIGATEK P/N GM92038 FOR INTHD SPRNG	1
12	99875308	MNL TECH REF MNL,SWIPE RDR W/3TK SPI INTHD	0

HEAD WIRING

PCB J1	SIGNAL	COLOR	P1, CONN
1	SCL	YELLOW	3
2	SDA	WHITE	4
3	VIN	RED	1
4	DAV	GREEN	5
5	GND	BLACK	2

REVISIONS			
REV	DESCRIPTION	DATE	INITIAL

NOTES: UNLESS OTHERWISE SPECIFIED
1. DIMENSIONS ARE IN MILLIMETERS (INCHES)
2. THE PCB 21030504 TO BE SOLDERED TO THE PARTIALLY EPOXY-FILLED HEAD, AND WIRES TO BE SOLDERED TO THE BOARD PRIOR TO APPLYING THE EPOXY. USE A 3:1 (1.2G TO .4G) RATIO OF WINKING EPOXY WK-571A AND HARDENER WK-571B TO FILL THE HEAD AND COVER THE PCB ASM.
3. WORKMANSHIP TO BE COMPLIANT WITH THE REQUIREMENTS OF IPC-A-610, CLASS 2.
4. WIRE:32AWG. TWIST WIRES @ 1-2 TURNS/INCH.
5. TERMINAL 50058-8100 MAY BE USED AS SUBSTITUTE.
6. P/b MARK TO BE LOCATED ON OR NEAR LABEL.

YELLOW J1-PIN 1
WHITE J1-PIN 2
RED J3-PIN 3
GREEN J4-PIN 4
BLK J5-PIN 5

TK3
TK2
TK1

CONNECTOR 5PIN FEM, JST P/N ZHR-5
TERMINALS CRIPM, JST-003T-PO.5 (X5)

ASM 21030023 REV X

JST-PIN 1 RED
P1

140.0±6.4
(5.51±2.5)

DIMENSIONS ARE IN MM(IN)
DATE 5/21/2008
DRAWN BY HL
DESIGNED BY
CHECKED BY

TOLERANCE:
X ±1.3 (.05)
XX ±.5 (.02)
XXX ±13 (.005)
ANGLES ±1°

MATERIAL:
FINISH:

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TITLE:
INTHD SPI INTHD 90MM 3TK W/140MM WRE,5PJST CONN

SIZE **B**
DWG. NO. **21030023**
REV **A.0003**
SCALE: 2
SHEET 1 OF 1

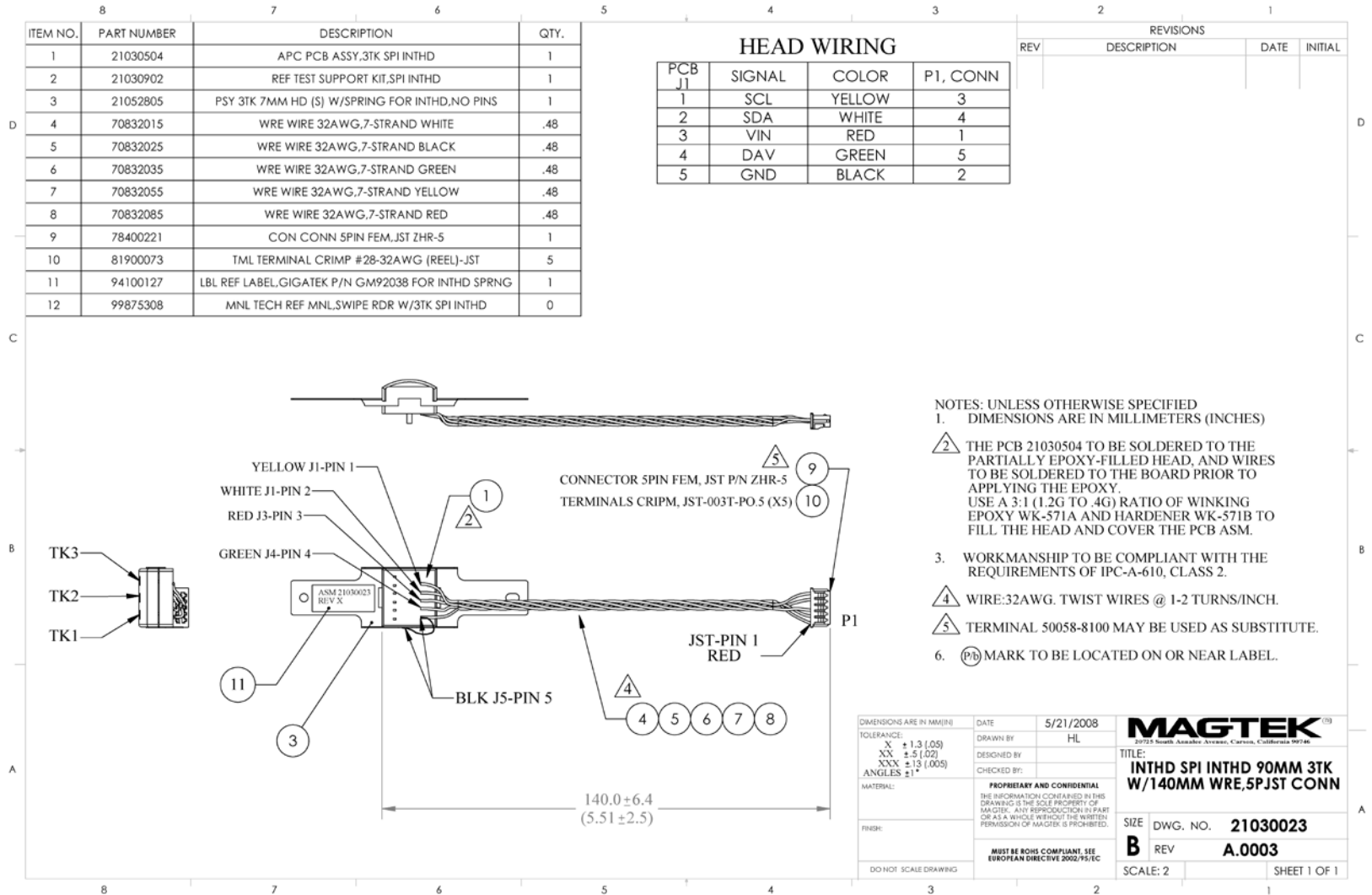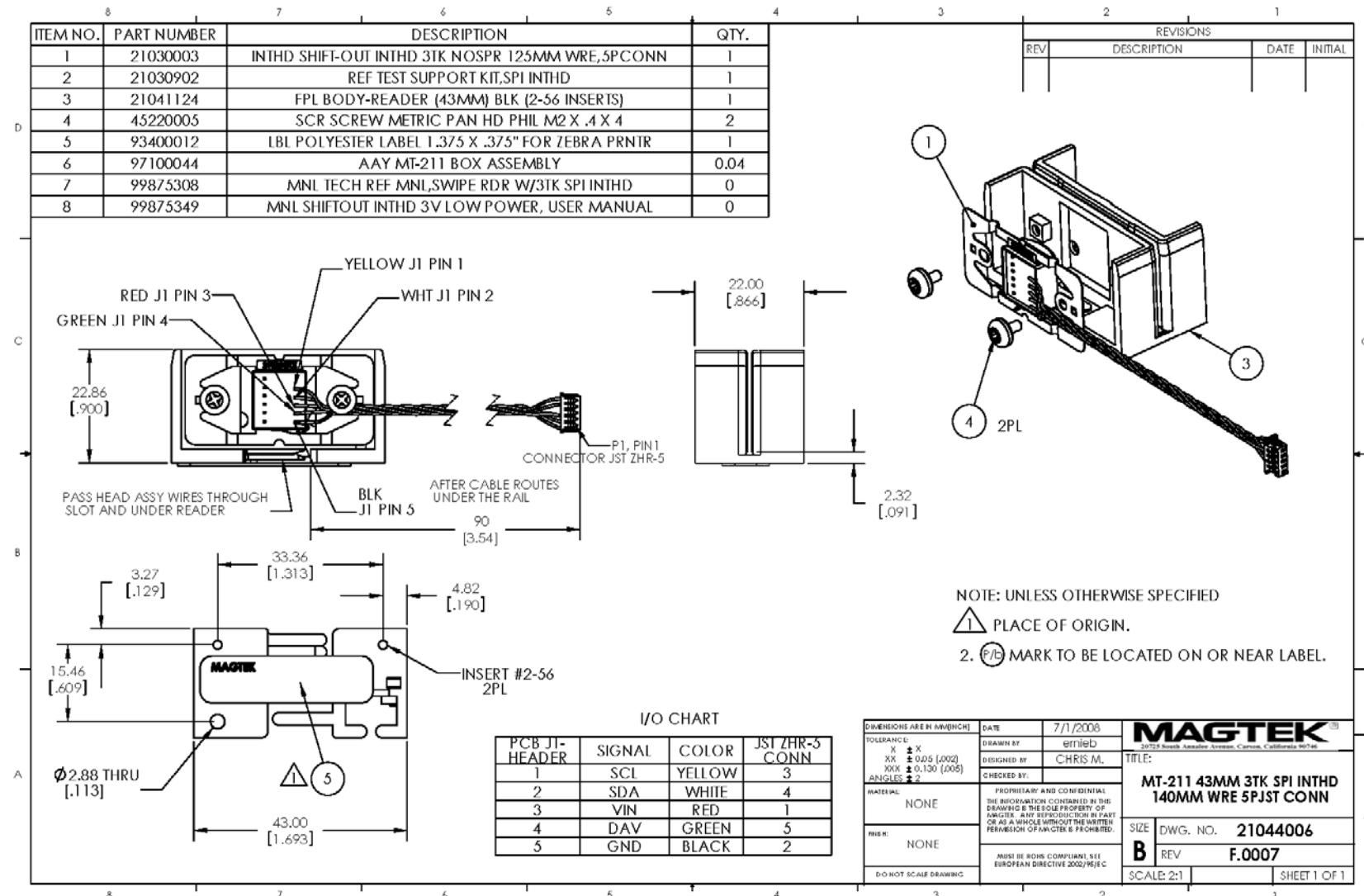**Figure B-1. 90mm Swipe Reader with 3-Track SPI IntelliHead**

Figure B-2. 43mm Swipe Reader with 3-Track SPI IntelliHead