TRIPLE-TRACK ASIC DEVELOPMENT PCB

TECHNICAL REFERENCE MANUAL

Manual Part Number 99875271-1

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MAGTEK®

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1710 Apollo Court
Seal Beach, CA 90740
Phone: (562) 546-6400
FAX: (562) 546-6301
Technical Support: (651) 415-6800
www.magtek.com

REVISIONS

Rev Number	Date	Notes
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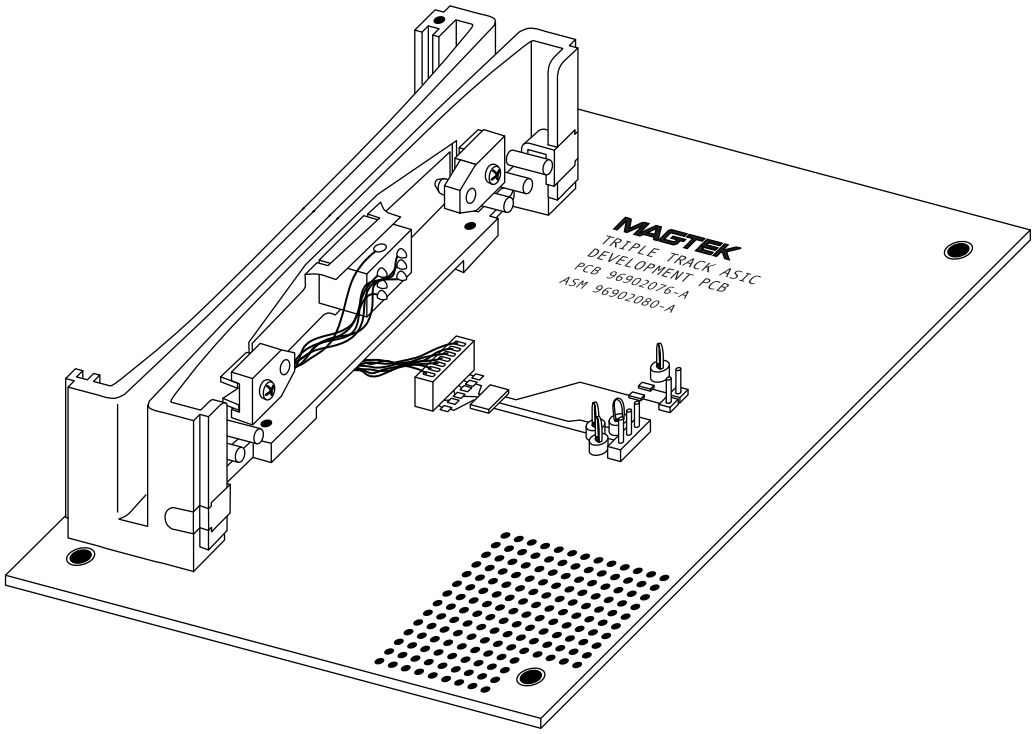

Figure 1. Triple-Track ASIC Development PCB.

OVERVIEW

The Triple-Track ASIC Development PCB may be used by MagTek customers to assist with the design, development, and integration of the MagTek Triple-Track ASIC into their own reader or terminal designs.

Typically this Development PCB will be used by electrical or firmware engineers, who need a "test platform" for developing electronics and firmware required to control the ASIC.

The Development PCB contains the following features:

- MagTek 3-track swipe reader chassis
- MagTek Triple-Track ASIC, Part Number 21006536
- J3 Header for supplying power
- J2 Header for connecting signals to the customer's microcontroller-based PCB
- Test points which allow easy connection of test probes to the J2 and J3 signals
- Vector-board area, which provides a convenient location for mounting/connecting external electronic components (if required).

Connecting the Development PCB to customer-supplied electronics will provide a convenient test platform that will allow the customer to develop required software interfaces and to perform read-reliability analysis.

Configuration

The part number of the Triple-Track ASIC Development PCB is 96901228.
The part number of the Triple-Track ASIC is 210065036.
The part number of the *Triple-Track ASIC with Shift-Out, Specifications* is 99875259.

RELATED DOCUMENTS

IMPORTANT:

The developer should be familiar with ***Triple-Track ASIC with Shift-Out, Specifications***, part number **99875259**, because this document provides all required electrical, mechanical, and software information to develop a working interface with the ASIC.

HELP/SUPPORT

MagTek is committed to providing technical support to assist with the integration of the MagTek Triple-Track ASIC. Please contact Mag-Tek Help Desk at (651) 415-6800 for assistance with any technical questions that may arise.

DIMENSIONS

The dimensions of the Development PCB are as follows:

Height: 5.0 in (127 mm)
Width: 4.0 in (102 mm)
Depth: 1.4 in (36 mm) (includes the height of the pads at the base of the PCB)
Weight: 2.7oz (76.6 g)

OPERATIONAL SETUP OF DEVELOPMENT PCB

Connectors and test points are shown in Figure 2. Follow the steps below:

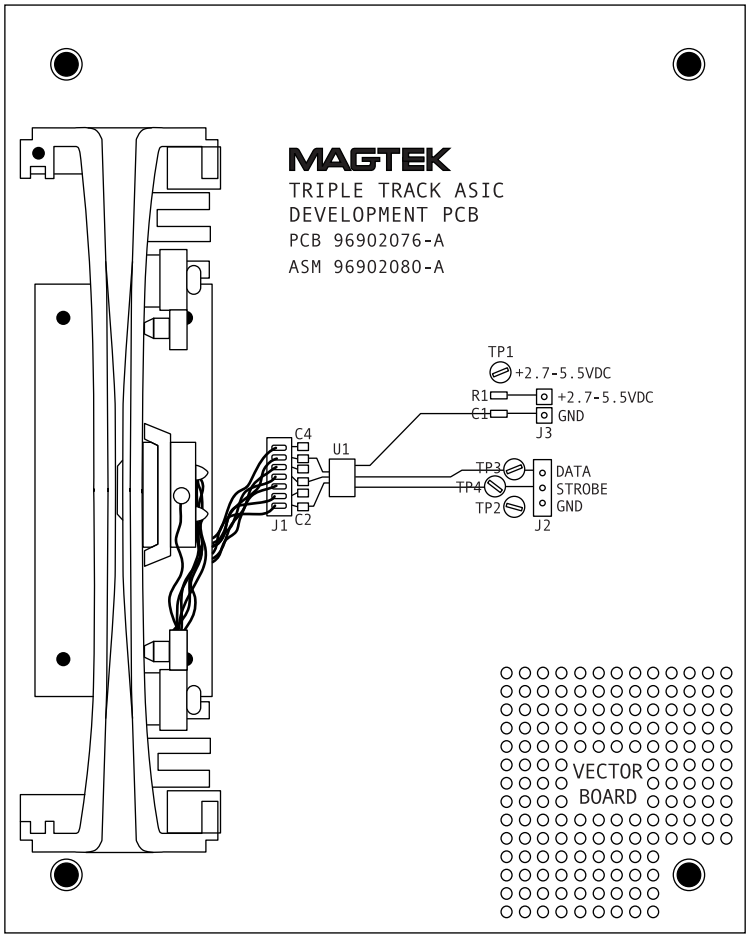

Figure 2. Connectors, Components, and Test Points

1. Connect the interface signals from the J2 connector, as indicated on the PCB silkscreen, to the customer-supplied electronics.

2. Connect the power to the J3 connector as indicated on the PCB silkscreen.

3. After power is applied, the user can then swipe a magstripe card through the reader and monitor the signals at the J2 header. After an encoded card is swiped, the Data line will transition low as a signal that the card has been read. At this time the customer's interface must begin the handshaking and data extraction routines as outlined in the Triple-Track ASIC specifications document part number 99875259.

4. User software can then be developed to move card data from the ASIC to the user's reader or terminal PCB.

CONNECTORS, COMPONENTS, AND TEST POINTS

Connectors, Components, and Test Points are shown in Figure 2.

Connectors and Test Points

Mating connectors for J2 and J3 can be any 0.10" center connector such as the Molex 2695 series.

J1 connects the signals from the magstripe reader to the Triple-Track ASIC.

J2 connects power, (+2.7 – 5.5 VDC (TP1) and Gnd from an external source to the Triple-Track ASIC Development PCB.

J3 connects DATA (TP3), which is the only *output* of the ASIC, STROBE (TP4), which is the handshaking and data extraction *input* of the ASIC, and GND (TP2) signals to customer interface.

Components

The magstripe read head sends signals to J1, which are then sent to U1, the Triple-Track ASIC, for processing, and are then sent to the test points and output connector J2.

Test Points

The test points are shown and silk-screened as shown in Figure 2.

Vector Board

The vector board is shown and labeled in Figure 2. This area is provides a convenient location for mounting/connecting external electronic components (if required for developing and testing user software).